In re application of	:	Ahmad
Appl. No.	:	09/397,952
Filed	:	September 17, 1999
For	:	FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION
Examiner	:	Steven H. Rao
Art Unit	:	2814

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Appeal Brief -- Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

November 13, 2003
(Date)

Tina Chen, Reg. No. 44,606

Mail Stop Appeal Brief -- Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is an Appellants' Brief to the Board of Patent Appeals:

(X) An Amendment Accompanying Appeal Brief in 5 pages.

(X) Fee for filing brief in the amount of $330 is enclosed.

(X) If applicant has not requested a sufficient extension of time and/or has not paid any other fee in a sufficient amount to prevent the abandonment of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 11-1410 for any fee which may be due. Please credit any overpayment to Deposit Account No. 11-1410.

(X) Return prepaid postcard.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Ahmad
Appl. No.	:	09/397,952
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ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES
APPELLANTS' BRIEF

Mail Stop Appeal Brief -- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the final rejection set forth in a final Office Action mailed June 17, 2003 in the above-captioned application.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

The present application was originally filed with Claims 1-28. Applicant canceled Claims 16-22 in a preliminary amendment. In an amendment accompanying a Request for

Continued Examination (RCE) application, Applicant canceled Claim 2. In a subsequent amendment, Applicant canceled Claims 4, 6, and 24. Claims 1, 3, 5, 7-15, 23, and 25-28 are thus pending in the present application and have been finally rejected in the Office Action dated June 17, 2003, which final rejection was affirmed by an Advisory Action dated September 24, 2003.

Accordingly, Claims 1, 3, 5, 7-15, 23, and 25-28 are the subject of this appeal. These claims are attached hereto as Appendix A.

IV. STATUS OF AMENDMENTS

Appellant submits an amendment (attached hereto as a separate paper) to correct formalities in the claims. The amendments to the claims do not alter the scope of the claims. Appellant respectfully requests that the amendments be entered prior to review of this appeal by the Board. The claims as they were finally rejected are attached hereto as Appendix A. The claims as proposed to be amended are attached hereto as Appendix B.

V. SUMMARY OF THE INVENTION

The present invention relates generally to techniques for improving hot carrier resistance of a transistor gate in a semiconductor substrate.

The scale of integration of semiconductor devices has increased significantly, and more devices have been positioned on smaller sized silicon substrates. As devices have become smaller, the channel length of the devices have become so small that functional problems result. In particular, source/drain punchthrough and hot electron susceptibility are two such problems. Source/drain punchthrough results in lack of gate control over the transistor and causes significant current leakages. This problem may be reduced by positioning antipunchthrough implants, such as Boron for n-channel devices and Phosphorous or Arsenic for p-channel devices, in the channel regions.

Hot electron susceptibility, which is defined as the injection of high energy electrons into the gate oxide layer and polysilicon forming the gate of the CMOS structure, severely reduces the threshold voltage of the transistor. Hot electron susceptibility may be reduced by oxidizing the gate edge next to the source and drain regions by a conventional source/drain reoxidation,

thereby rounding the gate edges and increasing the gate oxide thickness at the gate edges. However, in ULSI applications, the oxide is not a very good dielectric for the higher electric fields in these applications.

Lightly doped drain (LDD) structures are also used to overcome hot electron susceptibility. In a LDD structure, the source/drain regions are formed by implanting two different ions with different doping densities. A lightly doped region adjacent a channel region separates the channel region from a heavily doped drain region, and the lightly doped region significantly reduces the high electric field that causes hot electron injection into the gate oxide. However, ever-decreasing device dimensions have brought many constraints to conventional LDD process technologies.

A proper LDD drain should provide adequate hot-carrier protection for the device. Nitrogen implantation into the source/drain regions prior to formation of the sidewall spacer (SiO_2) has been used for this purpose. The implanted nitrogen atoms are then segregated at the interface between the substrate and by a low temperature treatment, thereby forming a silicon nitride layer under the sidewall spacer, which can suppress the hot electron injection. However, this technique limits the nitrogen atom segregation to the area under the sidewall spacer. Due to the high electric field strength, the structure cannot suppress the hot electron injection into the gate oxide as the nitrogen segregated area tends to only cover the region under the CVD deposited sidewall spacer.

The present invention provides a processing technique that is capable of reducing punchthrough and hot electron susceptibility in smaller devices. The claimed invention is a process that improves hot carrier resistance of a transistor gate by isolating the gate polysilicon with a nitride film. In the preferred process, nitrogen is implanted into the substrate and nitrogen doped regions 118 are formed in the source and drain regions 117 of the substrate 101. The source and drain regions are subsequently reoxidized to oxidize exposed portions of the gate polysilicon 112 and the source and drain regions 117. Under the oxidation conditions, a polysilicon bird's beak region 124 forms and nitrogen atoms diffuse into the gate region to form silicon nitride. During oxide growth, the oxide layer 130 can extend laterally under the polysilicon gate edges and form a wedge shaped oxide profile at the gate edges due to the particular sequence used. The diffusion of nitrogen atoms into the oxidized gate edges advantageously forms silicon nitride under the gate edges. As is well known, silicon nitride is an

excellent dielectric and therefore provides effective protection against current leakage into the gate polysilicon. *See* Specification at p. 5, lns. 13-27; and p. 6, lns. 3-14.

Each of the pending claims recites nitrogen implantation into a substrate with defined source/drain regions and a gate structure, followed by an oxidation step. For example, independent Claim 1 recites a process of forming a gate structure on a semiconductor substrate, comprising providing a semiconductor substrate having a channel region formed therein so as to define a source and drain region and a gate structure. The gate structure includes a gate dielectric positioned on the channel region and a conductive layer positioned on the gate dielectric. The process also includes implanting nitrogen into the substrate and conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting the nitrogen.

VI. ISSUES BEFORE THE BOARD

This appeal turns on whether the pending claims are properly rejected under 35 U.S.C. §103 as being unpatentable over Ahmad et al. (U.S. Patent No. 5,405,791) in view of Arai et al. (U.S. Patent No. 5,972,783).

VII. GROUPING OF CLAIMS

The pending claims stand or fall together. Each of the pending claims recite nitrogen implantation followed by an oxidation step.

Appellant reserves the right to separately argue, in subsequent continuing applications, the patentability of various dependent features not addressed herein.

VIII. APPELLANT'S ARGUMENT

In the final Office Action mailed June 17, 2003, the Examiner rejected all of the pending claims as being unpatentable under 35 U.S.C. §103(a) over Ahmad et al., U.S. Patent No. 5,405,791, in view of Arai et al., U.S. Patent No. 5,972,783. Each of the pending claims recites a process in which nitrogen implantation is followed by source/drain oxidation.

A. Examiner's asserted combinations do not provide *prima facie* case of obviousness

The Examiner bears the initial burden to establish and support *prima facie* obviousness. See In re Rinehart, 531 F.2d 1048, 189 U.S.P.Q. 143 (CCPA 1976). To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references or in the knowledge generally available among those of ordinary skill in the art, to modify the reference. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). "The references themselves, not the invention itself, must provide some teaching whereby the applicant's combination would have been obvious." In re Forman, 933 F.2d 982 (Fed. Cir. 1991); Heidelberger Druckmaschinen AG v. Hantscho Commercial Products, Inc., 21 F.3d 1068 (Fed. Cir. 1993). "Obviousness can not be established by hindsight combination to produce the claimed invention . . . . [I]t is the prior art itself, and not the applicant's achievement, that must establish the obviousness of the combination." In re Dance, 160 F.3d 1339 (Fed. Cir. 1998). "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); see also Ecolochem, Inc. v. Southern California Edison Co., 227 F. 3d 1361 (Fed. Cir. 2000).

It is well established that when a rejection for obviousness depends on a combination of elements disclosed in prior art references, there must be motivation to combine those particular elements in the prior art **as a whole**. "There must be evidence that 'a skilled artisan, confronted with the same problems as the inventors and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed.'" In re Rouffet, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); see also In re Werner Kotzab, 217 F.3d 1365, 1371, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

Appellant submits that the Examiner's asserted combinations fail to provide a *prima facie* case of obviousness. Although the Examiner may have supplied all of the individual elements of the independent claims, it is not sufficient to show *prima facie* obviousness. The Examiner has not shown any teaching or suggestion in the cited art to combine the individual elements ***in the manner claimed*** in the present invention. In particular, Appellant has recited a particular sequence of steps and the prior art does not teach or suggest this sequence.

The Examiner relies on *Ex parte Rubin*, 128 U.S.P.Q. 440 (Pat. Bd. App. 1959) and *In re Burhans*, 154 F.2d 690 (CCPA 1946) for the proposition that altering the order of method steps

shown in the prior art is not patentable unless the order of the steps recited in the claims produces unexpected or advantageous results. In this case, however, *Rubin* and *Burhans* are inapplicable as Applicant has specifically taught the advantages and differences in the operation of a sequence in which nitrogen implantation is followed by a thermal oxidation step, as set forth in the following excerpts from the specification as originally filed:

> Unlike prior art drive steps, however, ***oxidation*** of the substrate causes upward migration and consumption of silicon atoms from the implanted areas 118 (as well as from the gate poly 112) to form the oxide layer 130. This ***is accompanied by upward motion of implanted nitrogen atoms.*** The nitrogen concentration difference between the growing oxide layer and the implanted areas 118 provides the driving force for the reaction. Thus, the implanted nitrogen atoms migrate to the growing oxide layer 130 at the substrate surface and a silicon nitride layer 131 is formed over the implanted source/drain regions 11.

Specification at p. 6, lns. 24-31 (emphasis added).

> Significantly, the ***silicon nitride formation 131 also extends laterally at least partially under the gate poly 112 in the region of the GBB 124, due to mobility of atoms during the oxidation,*** and to form a nitride edge portion at least partially underlying the gate corner 127. The edge portion 133 may form only the oxide/substrate interface, as illustrated, or nitrogen atoms may diffuse through the growing oxide 130 to the gate poly 112. This laterally grown edge portion 133 effectively isolates the lower polysilicon gate edges 127 from the neighboring source/drain regions and thus ***effectively minimizes the high electric field induced current leakages into the gate poly*** 112. As previously mentioned, ***in prior art applications*** the conventional oxide spacer deposition and the following heat treatment ***tend to limit the nitride formation to the region under the deposited sidewall spacer.*** However, this limited prior art isolation fails to adequately protect the device against hot electron injection.
>
> Specification at p. 7, lns. 5-17 (emphasis added).

Appellant submits that the sequence of the steps recited in the pending claims produces unexpected and advantageous results over the methods described in Ahmad et al. and Arai et al. The Examiner has failed to acknowledge the specific sequence of steps recited in the pending

claims. Each of the pending claims recites a process in which nitrogen implantation is followed by source/drain oxidation.

Appellant submits that Arai et al. does not teach any source/drain reoxidation. The Examiner noted in the final Office Action that Arai et al. teaches source/drain oxidation at col. 12, lines 40-44 and 54-67. However, Appellant submits that Arai et al, at col. 12, lines 40-67, teaches diffusion of nitrogen ions "by an annealing treatment, whereby oxynitride layer 5a is formed at each edge of gate oxide film 2 and nitrogen diffusion layer 6a is formed in silicon substrate 1." Arai et al. teaches nitrogen implantation followed by an annealing treatment, rather than teaching source/drain reoxidation as recited in the pending claims.

Furthermore, as noted by the Examiner in the final Office Action, Ahmad et al. does not describe any nitrogen implantation into the semiconductor substrate. The previous paragraph clarifies that Arai et al. does not teach any source/drain oxidation. Since neither reference includes both steps, it is clear that the sequence of nitrogen implantation followed by source/drain oxidation is not taught or suggested by the references, either individually or in combination. Appellant submits that it is only in hindsight that a skilled artisan would apply the nitrogen implantation described by Arai et al. prior to Ahmad's source/drain reoxidation.

As the Federal Circuit has long held, "[b]efore the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." In re Jones, 21 U.S.P.Q.2d 1941, 1943-44 (Fed. Cir. 1992). Appellant submits that while Arai et al. teaches nitrogen implantation and Ahmad et al. teaches source/drain reoxidation, neither of the references teaches or suggests a combination of the steps or the particular sequence of the steps recited in the pending claims.

In addition to a suggestion to combine, the Examiner must show that the prior art provides a reasonable expectation that nitrogen implantation followed by source/drain reoxidation would be successful in forming a sidewall spacer for the purpose of improving hot carrier resistance of a transistor gate by isolating the gate polysilicon with a nitride film. The Examiner needs to show that the skilled artisan would have expected such a combination to succeed. "Both the suggestion [to combine] and the expectation of success must be founded in the prior art, not in the applicant's disclosure." In re Dow Chemical Co., 5 U.S.P.Q.2d 1529, 1530 (Fed. Cir. 1988). The Ahmad et al. and Arai et al. references fail to suggest that there is

any expectation of improving hot carrier resistance of a transistor gate by isolating the gate polysilicon with a nitride film by carrying out the steps in the specific sequence (nitrogen implantation followed by source/drain reoxidation) claimed in the pending claims.

B. Conclusion

In summary, Appellant submits that the Examiner's combination of prior art references is inappropriate when applied to the claims that are subject to this appeal and that Claims 1, 3, 5, 7-15, 23, and 25-28 are allowable over the art of record. To summarize, Appellant submits that Claims 1, 3, 5, 7-15, 23, and 25-28 are patentable over the art of record because: (1) the Examiner has not shown any teaching or suggestion in the prior art for the specific sequence of nitrogen implantation followed by source/drain oxidation; and (2) one or ordinary skill in the art would not have combined the Ahmad et al. and Arai et al. references to arrive at the present invention.

IX. APPENDIX A

Attached hereto as Appendix A is a copy of the finally rejected claims in the present case.

X. APPENDIX B

Attached hereto as Appendix B is a copy of the claims in the present case as proposed to be amended.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 13, 2003

By: _____

Tina Chen
Registration No. 44,606
Attorney of Record
Customer No. 20,995
(415) 954-4114

APPENDIX A
(Claims as finally rejected)

1. A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

implanting nitrogen into said substrate; and

conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting said nitrogen.

2. (Canceled)
3. The process of Claim 1, wherein said substrate comprises silicon.
4. (Canceled)
5. The process of Claim 4, wherein implanting said nitrogen comprises doping the substrate with greater than about 10^{12} nitrogen atoms.
6. (Canceled)
7. The process of Claim 1, wherein said conductive layer comprises polysilicon.
8. The process of Claim 1, wherein conducting said source/drain reoxidation comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer.
9. The process of Claim 1, conducting said source/drain reoxidation comprises forming a nitride layer on said semiconductor substrate.
10. The process of Claim 9, wherein said nitride layer laterally extends under at least a portion of said conductive layer.
11. The process of Claim 1, wherein said gate dielectric comprises silicon oxide.
12. The process of Claim 1, further comprising depositing a second sidewall spacer over the sidewall spacer.
13. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor substrate having a channel region formed therein so as to define a source region and a drain region and a gate structure comprised of an isolation layer positioned on said channel region and a conductive layer positioned on said isolation layer;

implanting nitrogen into said source and drain regions;

oxidizing a portion of said conductive layer adjacent said implanted source and drain regions to form an oxide space and a protective layer over said source and drain regions, said protective layer comprising said nitrogen and characterized by a dielectric constant higher than that of silicon oxide.

14. The process of Claim 13, wherein oxidizing said portion of said conductive layer comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer and said protective layer extending at least partially under said conductive layer.

15. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer having a channel region formed therein so as to define a source and drain region and a gate structure comprised of an isolation layer positioned over said channel region and a conductive layer positioned over said isolation layer;

forming a nitrogen-rich region by implanting nitrogen into said source and drain regions;

conducting an oxidation step after forming said nitrogen-rich region, thereby transforming a portion of said conductive layer adjacent said nitrogen-rich region into an oxide spacer and simultaneously combining a portion of said substrate with said nitrogen to form a nitride protective layer over said substrate; and

depositing a sidewall spacer over the oxide spacer.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions by nitrogen implantation;

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electrode injection into said gate electrode, wherein forming said silicon nitride film includes conducting a source/drain reoxidation after forming said nitrogen doped region.

24. (Canceled)

25. The process of Claim 23, further comprising double diffuse boron implanting said source and drain regions.

26. The process of Claim 23, further comprising:

depositing an insulating layer over said gate electrode; and

anisotropically etching said insulating layer to form sidewall spacers.

27. The process of Claim 23, further comprising source/drain implanting said source and drain regions.

28. The process of Claim 27, further comprising lightly doping said source and drain regions to grade a junction between said channel and said source and drain regions.

APPENDIX B

(Claims as proposed to be amended)

1. A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

implanting nitrogen into said substrate; and

conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting said nitrogen.

2. (Canceled)
3. The process of Claim 1, wherein said substrate comprises silicon.
4. (Canceled)
5. (Amended as Proposed) The process of Claim [4] 1, wherein implanting said nitrogen comprises doping the substrate with greater than about 10^{12} nitrogen atoms.
6. (Canceled)
7. The process of Claim 1, wherein said conductive layer comprises polysilicon.
8. The process of Claim 1, wherein conducting said source/drain reoxidation comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer.
9. (Amended as Proposed) The process of Claim 1, wherein conducting said source/drain reoxidation comprises forming a nitride layer on said semiconductor substrate.
10. The process of Claim 9, wherein said nitride layer laterally extends under at least a portion of said conductive layer.
11. The process of Claim 1, wherein said gate dielectric comprises silicon oxide.
12. The process of Claim 1, further comprising depositing a second sidewall spacer over the sidewall spacer.
13. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor substrate having a channel region formed therein so as to define a source region and a drain region and a gate structure comprised of an isolation layer positioned on said channel region and a conductive layer positioned on said isolation layer;

implanting nitrogen into said source and drain regions;

oxidizing a portion of said conductive layer adjacent said implanted source and drain regions to form an oxide space and a protective layer over said source and drain regions, said protective layer comprising said nitrogen and characterized by a dielectric constant higher than that of silicon oxide.

14. The process of Claim 13, wherein oxidizing said portion of said conductive layer comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer and said protective layer extending at least partially under said conductive layer.

15. A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer having a channel region formed therein so as to define a source and drain region and a gate structure comprised of an isolation layer positioned over said channel region and a conductive layer positioned over said isolation layer;

forming a nitrogen-rich region by implanting nitrogen into said source and drain regions;

conducting an oxidation step after forming said nitrogen-rich region, thereby transforming a portion of said conductive layer adjacent said nitrogen-rich region into an oxide spacer and simultaneously combining a portion of said substrate with said nitrogen to form a nitride protective layer over said substrate; and

depositing a sidewall spacer over the oxide spacer.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions by nitrogen implantation;

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electrode injection into said gate electrode, wherein forming said silicon nitride film includes conducting a source/drain reoxidation after forming said nitrogen doped region.

24. (Canceled)

25. The process of Claim 23, further comprising double diffuse boron implanting said source and drain regions.

26. The process of Claim 23, further comprising:

depositing an insulating layer over said gate electrode; and

anisotropically etching said insulating layer to form sidewall spacers.

27. The process of Claim 23, further comprising source/drain implanting said source and drain regions.

28. The process of Claim 27, further comprising lightly doping said source and drain regions to grade a junction between said channel and said source and drain regions.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Ahmad
Appl. No.	:	09/397,952
Filed	:	September 17, 1999
For	:	FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION
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November 13, 2003

(Date)

Tina Chen, Reg. No. 44,606

AMENDMENT ACCOMPANYING APPEAL BRIEF

Mail Stop Appeal Brief -- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant respectfully requests that the following claim amendments be entered to correct formalities in the above-captioned application prior to review by the Board of Patent Appeals and Interferences. The amendments merely address formality issues and place the application in better condition for appeal.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

Please amend Claims 5 and 9 as follows:

1. (Previously presented) A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

implanting nitrogen into said substrate; and

conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting said nitrogen.

2. (Canceled)

3. (Previously presented) The process of Claim 1, wherein said substrate comprises silicon.

4. (Canceled)

5. (Currently amended) The process of Claim **[[4]]** 1, wherein implanting said nitrogen comprises doping the substrate with greater than about 10^{12} nitrogen atoms.

6. (Canceled)

7. (Previously presented) The process of Claim 1, wherein said conductive layer comprises polysilicon.

8. (Previously presented) The process of Claim 1, wherein conducting said source/drain reoxidation comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer.

9. (Currently amended) The process of Claim 1, wherein conducting said source/drain reoxidation comprises forming a nitride layer on said semiconductor substrate.

10. (Original) The process of Claim 9, wherein said nitride layer laterally extends under at least a portion of said conductive layer.

11. (Original) The process of Claim 1, wherein said gate dielectric comprises silicon oxide.

12. (Original) The process of Claim 1, further comprising depositing a second sidewall spacer over the sidewall spacer.

13. (Previously presented) A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor substrate having a channel region formed therein so as to define a source region and a drain region and a gate structure comprised of an isolation layer positioned on said channel region and a conductive layer positioned on said isolation layer;

implanting nitrogen into said source and drain regions;

oxidizing a portion of said conductive layer adjacent said implanted source and drain regions to form an oxide space and a protective layer over said source and drain regions, said protective layer comprising said nitrogen and characterized by a dielectric constant higher than that of silicon oxide.

14. (Original) The process of Claim 13, wherein oxidizing said portion of said conductive layer comprises growing a bird's beak region extending laterally into a selected portion of said conductive layer and said protective layer extending at least partially under said conductive layer.

15. (Previously presented) A process of forming a gate structure on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer having a channel region formed therein so as to define a source and drain region and a gate structure comprised of an isolation layer positioned over said channel region and a conductive layer positioned over said isolation layer;

forming a nitrogen-rich region by implanting nitrogen into said source and drain regions;

conducting an oxidation step after forming said nitrogen-rich region, thereby transforming a portion of said conductive layer adjacent said nitrogen-rich region into an oxide spacer and simultaneously combining a portion of said substrate with said nitrogen to form a nitride protective layer over said substrate; and

depositing a sidewall spacer over the oxide spacer.

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Previously presented) A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions by nitrogen implantation;

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electrode injection into said gate electrode, wherein forming said silicon nitride film includes conducting a source/drain reoxidation after forming said nitrogen doped region.

24. (Canceled)

25. (Original) The process of Claim 23, further comprising double diffuse boron implanting said source and drain regions.

26. (Original) The process of Claim 23, further comprising:

depositing an insulating layer over said gate electrode; and

anisotropically etching said insulating layer to form sidewall spacers.

27. (Previously presented) The process of Claim 23, further comprising source/drain implanting said source and drain regions.

28. (Previously presented) The process of Claim 27, further comprising lightly doping said source and drain regions to grade a junction between said channel and said source and drain regions.

REMARKS

Claims 1, 3, 5, 7-15, 23, and 25-28 are pending in this application. Claims 5 and 9 have been amended to correct formalities. Applicant respectfully requests that these claim amendments be entered prior to review of this application by the Board of Patent Appeals and Interferences.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 13, 2003

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